

PB855+

Manual

Rev. 0.3

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0 History

Version	Changes
0.2	first release
0.3	<ul style="list-style-type: none">§ new picture form the web support form; C: 1.2§ update block diagram; C: 2.1§ new pinning USB / LAN / Audio; C: 4.7§ new drawings witch additional dimensions about the position of CPU and GMCH; C: 7

1 Preamble

1.1 Instructions for the Use of this Manual

Please read this manual carefully before you start with the installation of this hardware device. The following rules should absolutely be followed:

You must discharge your body from electric power before touching this board.

Tools you use must be discharged from electric power as well.

Please make sure that neither the board you want to install, nor the unit you want to install this board on, is energized before installation.

Please do not touch any devices or components on the board.

1.2 Technical Support

Technical support for this product you can get the following ways:

- By describing the problem directly, using the support sheet on our homepage.
www.embedded-logic.de
- By downloading the support sheet from our homepage, filling out and sending via email (support@embedded-logic.de) or fax (+49 8071 595857).

Please keep in mind that for the solution of the problem it is necessary to give us a detailed description as well as revision, BIOS version and serial number of the product.

1.3 Guarantee

Embedded-logic GmbH issues a guarantee of 24 months on the hardware. The guarantee period starts on the issuing date of the invoice ex works. Pieces, which were damaged demonstrably as a result of manufacturing or material defects, will be substituted or repaired according to the estimation of embedded-logic GmbH. Thus an extension of the guarantee period will not arise. Substitution-pieces will pass into embedded-logic GmbH properties. Any further claims against embedded-logic GmbH, especially claims for redhibitory actions, decrease in value or indemnification, are not constituted through this guarantee. In such cases any material will be delivered free of charges. If the unit needs to be transported for repair, this will occur at sender's risk and expense.

Excluded from guarantee services are:

- Damages resulting from the interference of people not authorised by embedded-logic GmbH.
- Units with destroyed or removed serial number.
- Damages which result from the non-observance of instructions, such as the connection of a wrong voltage or electric current, careless treatment or misemployment of defect or out-of-date batteries as well as mistakes in the reverse poling of cables.
- Wear parts, for example damaged connectors
- Improper packing and improper additional packing

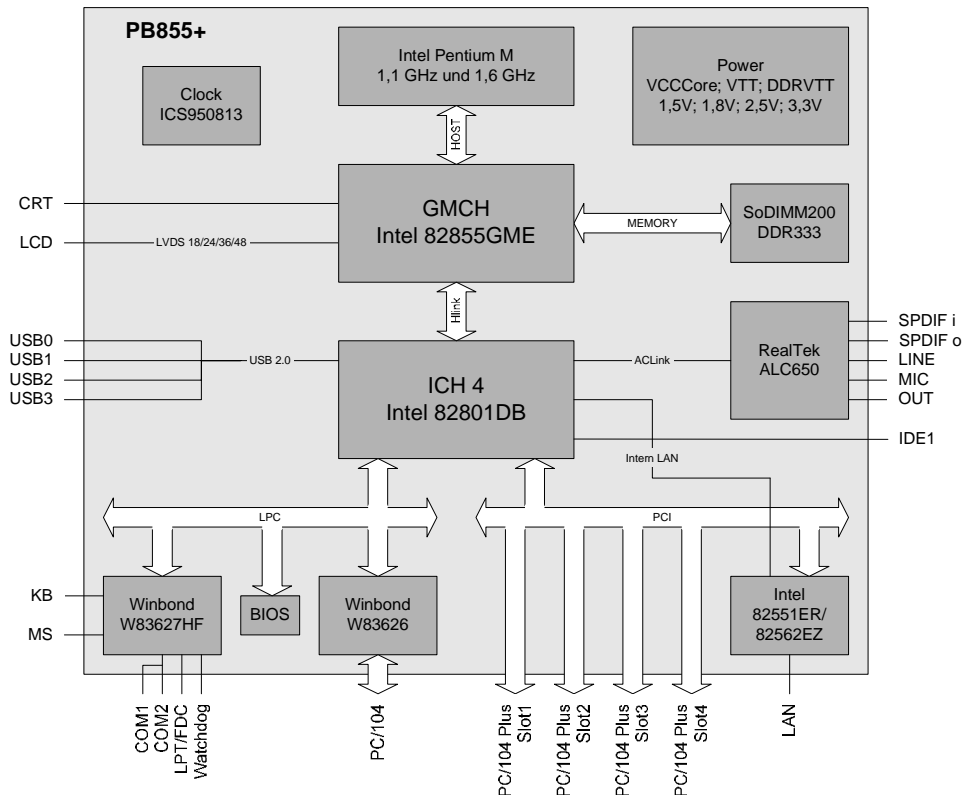
The guarantee refers to the first buyer and it is not transferable.

Before the unit is sent back for repair, a RMA number **must** be requested at embedded-logic GmbH to register the process.

2 Overview

2.1 Standard Features

The PB855+ is a highly complex PC/104 board with the functionalities of a motherboard. It is equipped with an Intel Pentium M CPU, 1GByte DDR-RAM memory capacity via SoDIMM200, PCI and ISA bus and additional peripheral devices such as two serial interfaces, one printer interface, floppy connection, LAN connection, Audio in and out, four USB interfaces, CRT, TFT and IDE connection.



- Processor Intel Pentium M 1,1GHz up to 1,6GHz
- Chipset Intel 855GME and Intel ICH4
- DDR-RAM via SoDIMM200 up to 1 GByte PC333 with ECC
- Two serial interfaces COM1 up to COM2 (TTL/RS232)
- One parallel interface LPT1
- Ethernet 10/100BaseT
- Floppy interface via LPT
- One IDE interface
- PS/2 Keyboard / Mouse interface
- Four USB 2.0 interfaces
- AWARD BIOS 6.10
- CRT Connection
- TFT Connection, LVDS 18/24/36/48Bit
- AC97 compatible sound controller with SPDIF in and out
- RTC with external CMOS Battery
- 5V single supply voltage
- ISA via PC/104 connector
- PCI via PC/104-Plus connector
- Size 96 mm x 90 (115) mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation the following documents, specifications and web-pages were used and are recommended:

- ISA specification
IEEE996P
www.ieee.org
- PC/104 specification
Version 2.5
www.pc104.org
- PC/104-Plus specification
Version 2.0
www.pc104.org
- PCI specification
Version 2.3
www.pcisig.com
- ACPI specification
Version 2.0
www.acpi.info
- ATA/ATAPI specification
Version 7 Rev. 1
www.t13.org
- SM-bus specification
Version 1.0
www.smbus.org
- Intel chip description
855GM/GME datasheet, design guide
www.intel.com
- Intel chip description
ICH4 Datasheet
www.intel.com
- Winbond Chip description
W83627HF datasheet, W83626 datasheet
www.winbond-usa.com or www.winbond.com.tw
- Intel chip description
82551ER datasheet
www.intel.com
- Intel chip description
82562EZ datasheet
www.intel.com
- ICS chip description
ICS950813 datasheet
www.icst.com

2.3 Trade Marks

All trade marks are accepted.

3 Detailed Description

3.1 Power Supply

The power supply of the hardware module is effected via the power connector.

The board only requires an operating voltage of 5 volt \pm 5%, it is not necessary to connect all indicated voltages. Additional voltages may only be necessary for PC/104 expansion cards.

For safety reasons it is recommended to connect all power pins of the PC/104 connector to the power supply as well.

3.2 CPU

An Intel Pentium M processor is employed on the board. The package type allows a maximum DIE temperature of 100 degree Celsius and accords highest possible security even in rough environment.

The processor includes a second level cache of 1 MByte.

Furthermore the processors dispose of features known from the desktop range such as MMX2, serial number, loadable microcode etc. .

3.3 Memory

Conventional SoDIMM200 memory modules are employed on the PB855+ boards, which are typically employed in notebooks. Because of its high complexity it is possible, that for mechanical reasons not all kinds of memory modules can be employed. Please ask your distributor for recommended memory modules.

With SoDIMM modules, that are actually available, a memory extension up to 1 GB is possible.

All timing parameters for different memories are automatically set by BIOS.



Attention

For higher security demands SoDIMM modules with ECC parity checking are available. The BIOS will use this option automatically, though it can be manually disabled in setup. You may notice a performance decrease with ECC enabled, when using higher video resolutions.

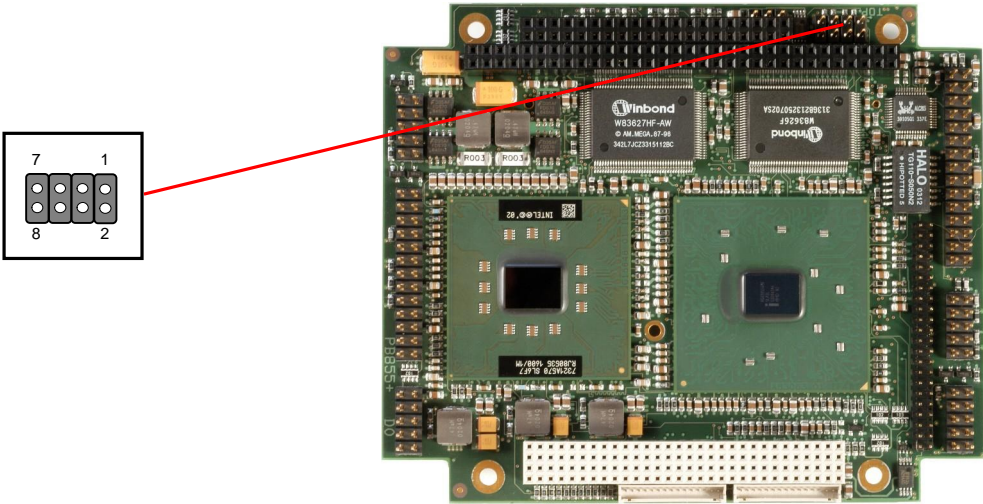
4 Connectors

4.1 Power Supply

The connector for the power supply is a standard IDC socket connector with a spacing of 2.54 mm.

The board only requires an operating voltage of 5 volt ± 5%, it is not necessary to connect all indicated voltages. Additional voltages may only be necessary for PC/104 expansion cards.

For safety reasons it is recommended to connect all power pins of the PC/104 connector to the power supply as well.

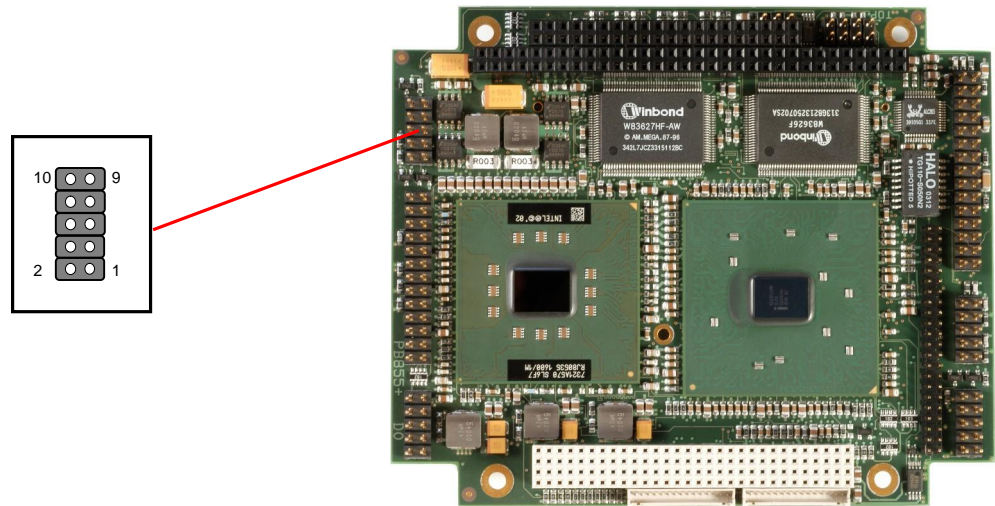


Description	Name	Pin		Name	Description
ground	GND	1	2	VCC	5V supply
CMOS Batterie ≥ 3Volt	VBAT	3	4	12V	12V supply
-5V supply	-5V	5	6	-12V	-12V supply
ground	GND	7	8	VCC	5V supply

4.2 System

The system connector, which has the main functions that are necessary to start the board, is provided via a standard IDC socket connector with a spacing of 2.54 mm.

This connector supports the following interfaces: PS/2 keyboard, PS/2 mouse, speaker, external RTC-battery, hard disk LED and reset of the board.

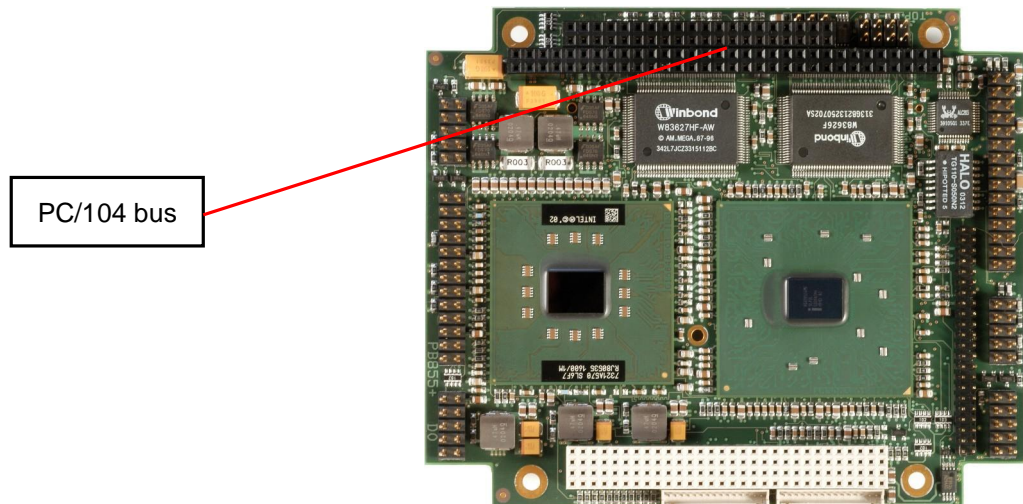


Description	Name	Pin		Name	Description
speaker to 5V	SPEAKER	1	2	GND	ground
reset to ground	RESET#	3	4	KLOCK#	keyboard lock
keyboard Data	KDAT	5	6	KCLK	keyboard clock
mouse data	MDAT	7	8	MCLK	mouse clock
CMOS battery ≥ 3 volt	VBAT	9	10	VCC	5 volt

4.3 PC/104 Bus

An onboard LPC to ISA-bridge makes it possible to expand the functionality of the board with additional PC/104 cards.

Because of the transformation from LPC to ISA it is unfortunately not possible to realize a 16Bit access. This does not mean that these cards cannot be used, but the 16Bit access is divided into two accesses. Therefore the access to these cards is a little bit slower. Unfortunately recent chipsets do not offer ISA buses any more, so this is the only universal solution that can be offered.



Pinning of the standard 8Bit PC/104 connector.

Description	Name	Pin	Name	Description
IO channel check	IOCHK#	A1	B1	GND
ISA – data 7	SD7	A2	B2	RSTDRV
ISA – data 6	SD6	A3	B3	VCC
ISA – data 5	SD5	A4	B4	IRQ9
ISA – data 4	SD4	A5	B5	-5V
ISA – data 3	SD3	A6	B6	DRQ2
ISA – data 2	SD2	A7	B7	-12V
ISA – data 1	SD1	A8	B8	IOCHRDY
ISA – data 0	SD0	A9	B9	12V
ISA – IO channel ready	IOCHRDY	A10	B10	Reserved
ISA – address enable	AEN	A11	B11	SMEMW#
ISA – address 19	SA19	A12	B12	SMEMR#
ISA – address 18	SA18	A13	B13	IOW#
ISA – address 17	SA17	A14	B14	IOR#
ISA – address 16	SA16	A15	B15	DACK3#
ISA – address 15	SA15	A16	B16	DRQ3
ISA – address 14	SA14	A17	B17	DACK1#
ISA – address 13	SA13	A18	B18	DRQ1
ISA – address 12	SA12	A19	B19	REFRESH#
ISA – address 11	SA11	A20	B20	SYSCLK
ISA – address 10	SA10	A21	B21	IRQ7
ISA – address 9	SA9	A22	B22	IRQ6
ISA – address 8	SA8	A23	B23	IRQ5
ISA – address 7	SA7	A24	B24	IRQ4
ISA – address 6	SA6	A25	B25	IRQ3
ISA – address 5	SA5	A26	B26	DACK2#
ISA – address 4	SA4	A27	B27	T/C

Description	Name	Pin		Name	Description
ISA – address 3	SA3	A28	B28	BALE	ISA – address latch en.
ISA – address 2	SA2	A29	B29	VCC	5V supply
ISA – address 1	SA1	A30	B30	OSC	ISA – 14,318MHz
ISA – address 0	SA0	A31	B31	GND	ground
ground	GND	A32	B32	GND	ground

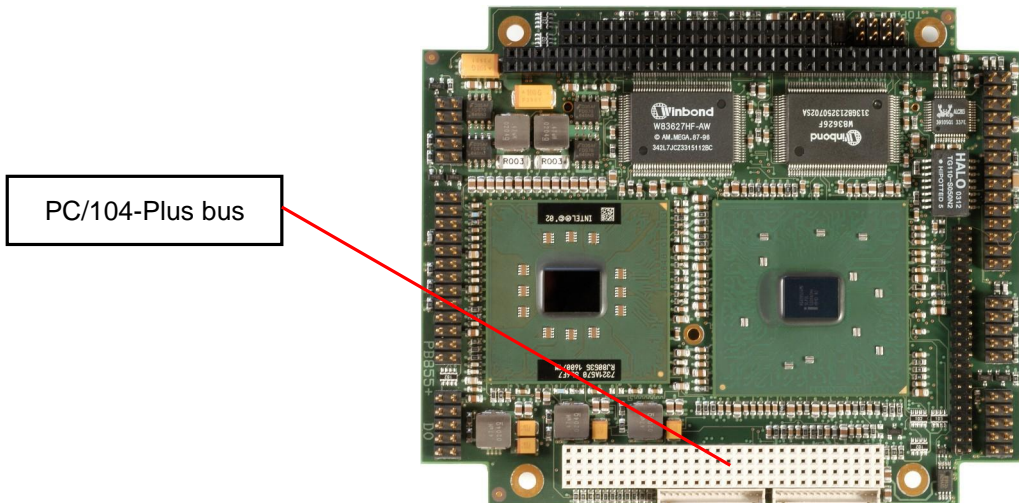
Pinning of the 16Bit expansion PC/104 connector.

Description	Name	Pin		Name	Description
ground	GND	C0	D0	GND	ground
ISA – byte High Enable	SBHE#	C1	D1	MEMCS16#	ISA – memory chip select
ISA – latched Address 23	LA23	C2	D2	IOCS16#	ISA – IO chip select
ISA – latched Address 22	LA22	C3	D3	IRQ10	ISA – interrupt 10
ISA – latched Address 21	LA21	C4	D4	IRQ11	ISA – interrupt 11
ISA – latched Address 20	LA20	C5	D5	IRQ12	ISA – interrupt 12
ISA – latched Address 19	LA19	C6	D6	IRQ15	ISA – interrupt 15
ISA – latched Address 18	LA18	C7	D7	IRQ14	ISA – interrupt 14
ISA – latched Address 17	LA17	C8	D8	DACK0#	ISA – DMA acknowledge 0
ISA – memory Read	MEMR#	C9	D9	DRQ0	ISA – DMA request 0
ISA – memory Write	MEMW#	C10	D10	DACK5#	ISA – DMA acknowledge 5
ISA – data 8	SD8	C11	D11	DRQ5	ISA – DMA request 5
ISA – data 9	SD9	C12	D12	DACK6#	ISA – DMA acknowledge 6
ISA – data 10	SD10	C13	D13	DRQ6	ISA – DMA request 6
ISA – data 11	SD11	C14	D14	DACK7#	ISA – DMA acknowledge 7
ISA – data 12	SD12	C15	D15	DRQ7	ISA – DMA request 7
ISA – data 13	SD13	C16	D16	VCC	5V supply
ISA – data 14	SD14	C17	D17	MASTER#	ISA – bus master
ISA – data 15	SD15	C18	D18	GND	ground
	reserved	C19	D19	GND	ground

4.4 PC/104-Plus Bus

The PC/104-Plus connector is used for expansion cards, e. g. SCSI, IEEE1394 etc. . A maximum of four PC/104-Plus cards are supported.

The interrupt routing and the IDSEL signals for the expansion cards are specified in the PC/104-Plus specification.

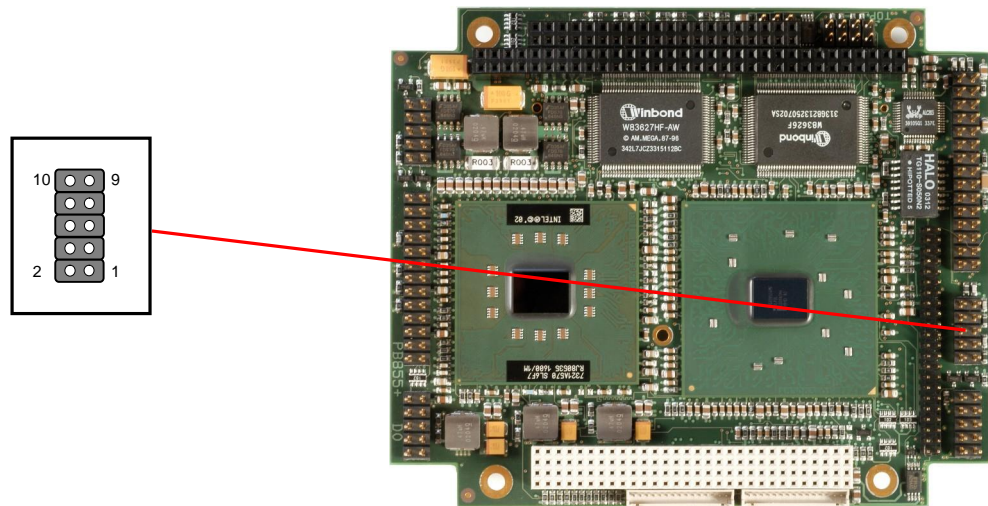


Description	Name	Pin	Name	Description
ground	GND	A1	B1	reserved
5 volt – IO-buffer power	VCCIO	A2	B2	AD2
PCI – address/data 5	AD5	A3	B3	GND
PCI – com/byte enable 0	CBE0#	A4	B4	AD7
Ground	GND	A5	B5	AD9
PCI – address/data 11	AD11	A6	B6	VCCIO
PCI – address/data 14	AD14	A7	B7	AD13
3,3 volt	3,3V	A8	B8	CBE1#
PCI – system error	SERR#	A9	B9	GND
ground	GND	A10	B10	PERR#
PCI – stop	STOP#	A11	B11	3,3V
3,3 volt	3,3V	A12	B12	TRDY#
PCI – frame	FRAME#	A13	B13	GND
ground	GND	A14	B14	AD16
PCI – address/data 18	AD18	A15	B15	3,3V
PCI – address/data 21	AD21	A16	B16	AD20
3,3 volt	3,3V	A17	B17	AD23
PCI – ID select slot 1	IDSEL0	A18	B18	GND
PCI – address/data 24	AD24	A19	B19	CBE3#
ground	GND	A20	B20	AD26
PCI – address/data 29	AD29	A21	B21	VCC
5 volt supply	VCC	A22	B22	AD30
PCI – bus request slot 1	REQ0#	A23	B23	GND
ground	GND	A24	B24	REQ2#
PCI – bus grant slot 4	GNT1#	A25	B25	VCCIO
5 volt supply	VCC	A26	B26	CLK0
PCI – clock slot 3	CLK2	A27	B27	VCC
Ground	GND	A28	B28	INTD#
12 volt	12V	A29	B29	INTA#
-12 volt	-12V	A30	B30	REQ3#
				PCI – bus request slot 4

Description	Name	Pin		Name	Description
5 volt supply	VCC	C1	D1	AD0	PCI – address/data 0
PCI – address/data 1	AD1	C2	D2	VCC	5 volt supply
PCI – address/data 4	AD4	C3	D3	AD3	PCI – address/data 3
ground	GND	C4	D4	AD6	PCI – address/data 6
PCI – address/data 8	AD8	C5	D5	GND	ground
PCI – address/data 10	AD10	C6	D6	M66EN	PCI – 66MHz enable
ground	GND	C7	D7	AD12	PCI – address/data 12
PCI – address/data 15	AD15	C8	D8	3,3V	3,3 volt
	reserved	C9	D9	PAR	PCI – parity bit
3,3 volt	3,3V	C10	D10	Reserved	
PCI – lock	LOCK#	C11	D11	GND	ground
Ground	GND	C12	D12	DEVSEL#	PCI – device select
PCI – initiator ready	IRDY#	C13	D13	3,3V	3,3 volt
3,3 volt	3,3V	C14	D14	CBE2#	PCI – com/byte enable 2
PCI – address/data 17	AD17	C15	D15	GND	ground
ground	GND	C16	D16	AD19	PCI – address/data 19
PCI – address/data 22	AD22	C17	D17	3,3V	3,3 volt
PCI – ID select slot 2	IDSEL1	C18	D18	IDSEL2	PCI – ID select slot 3
5 volt – IO-buffer power	VCCIO	C19	D19	IDSEL3	PCI – ID select slot 4
PCI – address/data 25	AD25	C20	D20	GND	ground
PCI – address/data 28	AD28	C21	D21	AD27	PCI – address/data 27
ground	GND	C22	D22	AD31	PCI – address/data 31
PCI – bus request slot 2	REQ1#	C23	D23	VCCIO	5 volt – IO-buffer power
5 volt supply	VCC	C24	D24	GNT0#	PCI – bus grant slot 1
PCI – bus grant slot 3	GNT2#	C25	D25	GND	ground
ground	GND	C26	D26	CLK1	PCI – clock slot 2
PCI – clock slot 4	CLK3	C27	D27	GND	ground
5 volt supply	VCC	C28	D28	RST#	PCI – reset
PCI – interrupt B	INTB#	C29	D29	INTC#	PCI – interrupt C
PCI – bus grant slot 4	GNT3#	C30	D30	GND	ground

4.5 VGA

The CRT-VGA signals are provided by a standard IDC socket connector with a spacing of 2.54 mm. This interface allows the connection of a standard VGA-monitor.



Description	Name	Pin	Name	Description
analog red	RED	1	2	GND
analog green	GREEN	3	4	DDDA
analog blue	BLUE	5	6	DDCK
vertical sync	VSYNC	7	8	GND
horizontal sync	HSYNC	9	10	GND

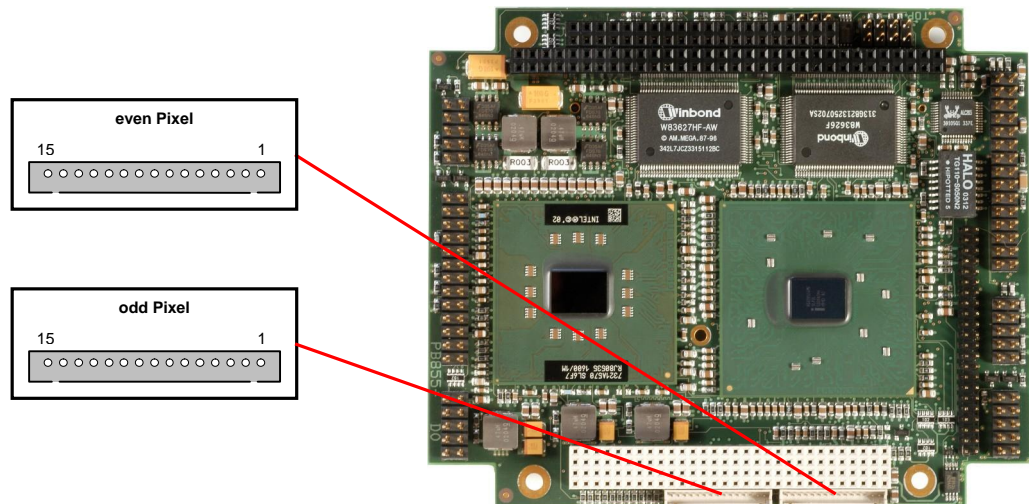
4.6 LCD

The LCD is connected via two 15 pin connectors from Hirose (www.hirose.com DF13 serie). The power supply for the display is also provided through these connectors.

The PB855+ board only supports displays with LVDS interface. For displays with digital interface an extra receiver board is available. There is no support for DSTN displays.

With the LVDS interface it is possible to trigger LVDS displays with a maximum of 24Bit colour depth and one or two pixels per clock. For single pixel displays only one connector is necessary.

The display type can be chosen over the BIOS setup.



The following table shows the pin description for even pixels. For display with single pixel interface only this connector is necessary.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	TXO00-	LVDS even data 0 -
4	TXO00+	LVDS even data 0 +
5	TXO01-	LVDS even data 1 -
6	TXO01+	LVDS even data 1 +
7	TXO02-	LVDS even data 2 -
8	TXO02+	LVDS even data 2 +
9	TXO0C-	LVDS even clock -
10	TXO0C+	LVDS even clock +
11	TXO03-	LVDS even data 3 -
12	TXO03+	LVDS even data 3 +
13	BL_VCC	switched 5 volt for backlight
14	FP_3,3V	switched 3,3 volt for display
15	FP_3,3V	switched 3,3 volt for display

The following table shows the pin description for odd pixels. For displays with dual pixel interface both connectors are necessary.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	TXO10-	LVDS odd Data 0 -
4	TXO10+	LVDS odd Data 0 +
5	TXO11-	LVDS odd Data 1 -
6	TXO11+	LVDS odd Data 1 +
7	TXO12-	LVDS odd Data 2 -
8	TXO12+	LVDS odd Data 2 +
9	TXO1C-	LVDS odd Clock -
10	TXO1C+	LVDS odd Clock +
11	TXO13-	LVDS odd Data 3 -
12	TXO13+	LVDS odd Data 3 +
13	LCD-CLK	I2C bus clock for LCD ¹
14	LCD-DAT	I2C bus data for LCD ¹
15	VCC	5 volt

¹ This function is currently not supported.

4.7 USB 1 to 4, LAN and Audio

The connector for USB 1 to 4, LAN and sound use a standard IDC socket connector with a spacing of 2.54 mm.

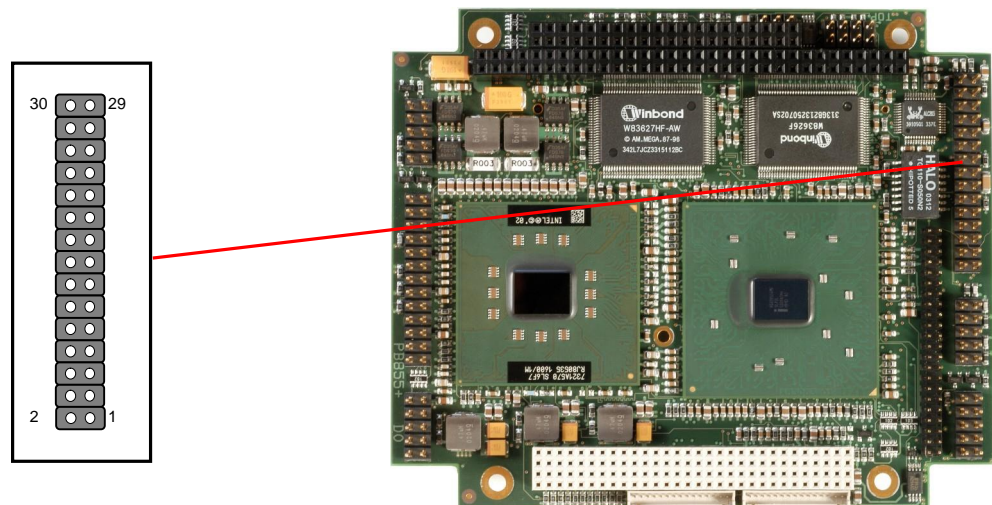
Necessary settings can be accomplished in BIOS setup.

All USB-channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with an USB keyboard without enabling USB keyboard support. Running windows with these features enabled may lead to significant performance or functionality limitations. Every USB interface provides up to 500 mA current and is protected by an electronic fuse.

The LAN-interface supports 10BaseT and 100BaseT compatible net components with automatic bandwidth selection. Additional signals are provided for status LEDs.

Additionally on this plug one can also find signals for Audio input and output. These Audio in and output have dual functionality. Default functionality is Audio in and out. OS dependant device drivers can switch all of these signals to support an 5.1 output; thus in this mode no Audio input signals are available.

Signals "SPDIFI" and "SPDIFO" provide digital input and output. Necessary transformation to Coax or optical must be performed externally.

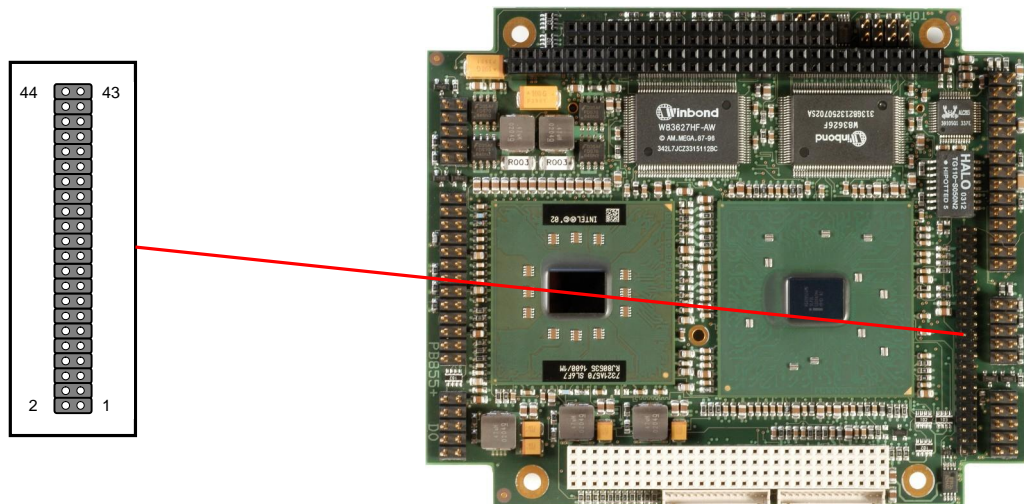


Description	Name	Pin	Name	Description
5 volt for USB1	USB1 VCC	1	2	USB2 VCC
USB- channel 1	USB1-	3	4	USB2-
USB+ channel 1	USB1+	5	6	USB2+
ground	GND	7	8	GND
USB+ channel 3	USB3+	9	10	USB4+
USB- channel 3	USB3-	11	12	USB4-
5 volt for USB3	USB3 VCC	13	14	USB4 VCC
LAN activity	ACTLED	15	16	SPEEDLED
LAN RX+	LANRX+	17	18	LANTX+
LAN RX-	LANRX-	19	20	LANTX-
digital output SPDIF	SPDIFO	21	22	3,3V
digital input SPDIF	SPDIFI	23	24	S_AGND
sound output right / frond output right	LOUT_R / FRONT_R	25	26	LOUT_L / FRONT_L
AUX output right / rear output right	AUXA_R / REAR_R	27	28	AUXA_L / REAR_L
microphone input 1 / center output	MIC1 / CENTER	29	30	MIC2 / LFE

4.8 IDE Interface

The primary IDE interface is a standard IDC socket connector with a spacing of 2 mm. All commercial IDE devices are supported. An adapter for a spacing of 2.54 mm is necessary.

The required settings are made in the BIOS setup.



Description	Name	Pin	Name	Description
reset	PRST#	1	2	GND
data bit 7	PDD7	3	4	PDD8
data bit 6	PDD6	5	6	PDD9
data bit 5	PDD5	7	8	PDD10
data bit 4	PDD4	9	10	PDD11
data bit 3	PDD3	11	12	PDD12
data bit 2	PDD2	13	14	PDD13
data bit 1	PDD1	15	16	PDD14
data bit 0	PDD0	17	18	PDD15
ground	GND	19	20	reserved
DMA request signal	PDDREQ	21	22	GND
write signal	PDIOW#	23	24	GND
read signal	PDIOR#	25	26	GND
ready signal	PDRDY	27	28	reserved
DMA acknowledge signal	PDDACK#	29	30	GND
interrupt signal	PDIRQ	31	32	reserved
address bit 1	PDA1	33	34	PDIAG#
address bit 2	PDA0	35	36	PDA2
chip select signal 0	PDSC0#	37	38	PDCS1#
device active	DASP#	39	40	GND
supply HDD 5V	VCC	41	42	VCC
ground	GND	43	44	Reserved

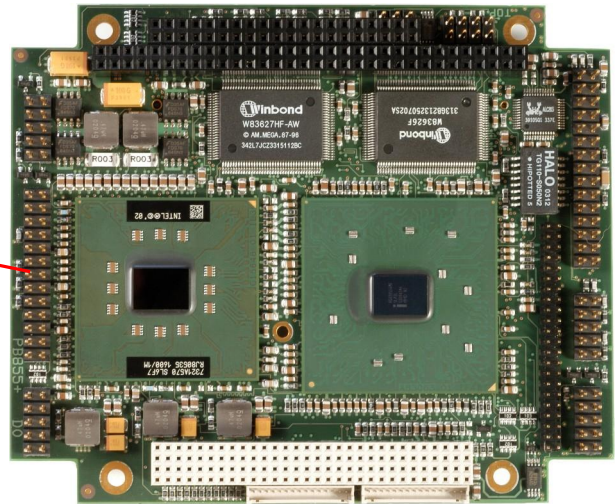
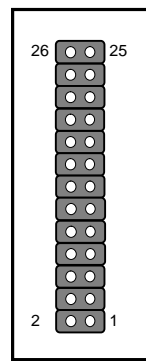
4.9 Parallel Interface LPT

The parallel interface is a standard IDC socket connector with a spacing of 2.54 mm.

The port address and the interrupt are set via the BIOS setup.

Floppy drives can be connected to this interface as well. For that purpose this function is enabled via BIOS setup. A floppy drive is connected with a special cable.

Please ask your distributor for such a cable.



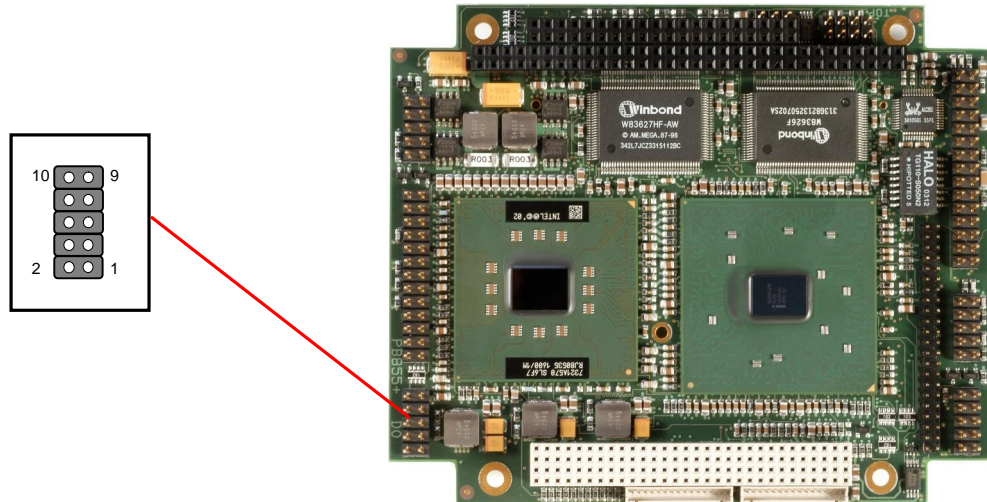
Description	Name	Pin		Name	Description
strobe	STB#	1	2	AFD#	automatic line feed
line printer data 0	PD0	3	4	ERR#	error
line printer data 1	PD1	5	6	INIT#	init
line printer data 2	PD2	7	8	SLIN#	select input
line printer data 3	PD3	9	10	GND	ground
line printer data 4	PD4	11	12	GND	ground
line printer data 5	PD5	13	14	GND	ground
line printer data 6	PD6	15	16	GND	ground
line printer data 7	PD7	17	18	GND	ground
acknowledge	ACK#	19	20	GND	ground
busy	BUSY	21	22	GND	ground
paper end	PE	23	24	GND	ground
select printer	SLCT	25	26	VCC	5 volt

4.10 Serial Interface COM1

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm.

According to the product order, TTL level signals or RS232 standard signals are provided.

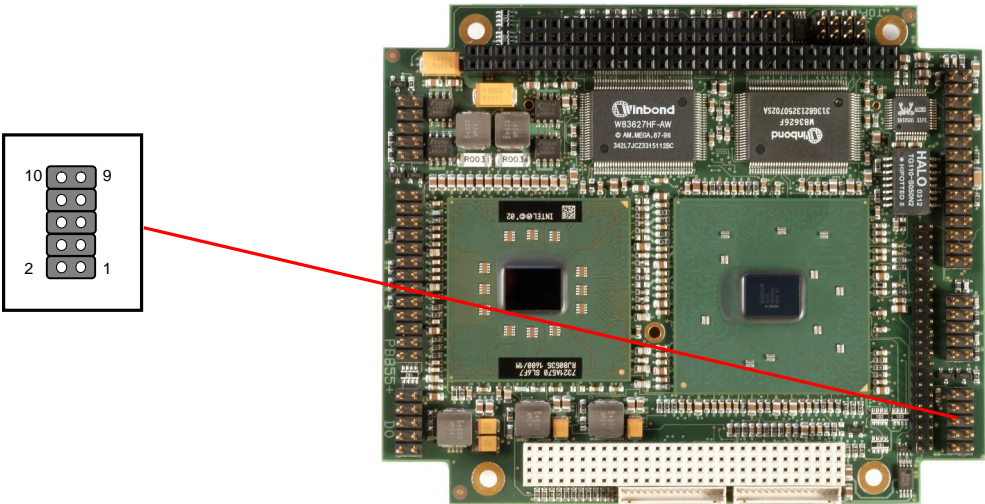
The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt

4.11 Serial Interface COM2

The serial interface is a standard IDC socket connector with a spacing of 2.54 mm. According to the product order, TTL level signals or RS232 standard signals are provided. The port address and the interrupt are set via the BIOS setup.

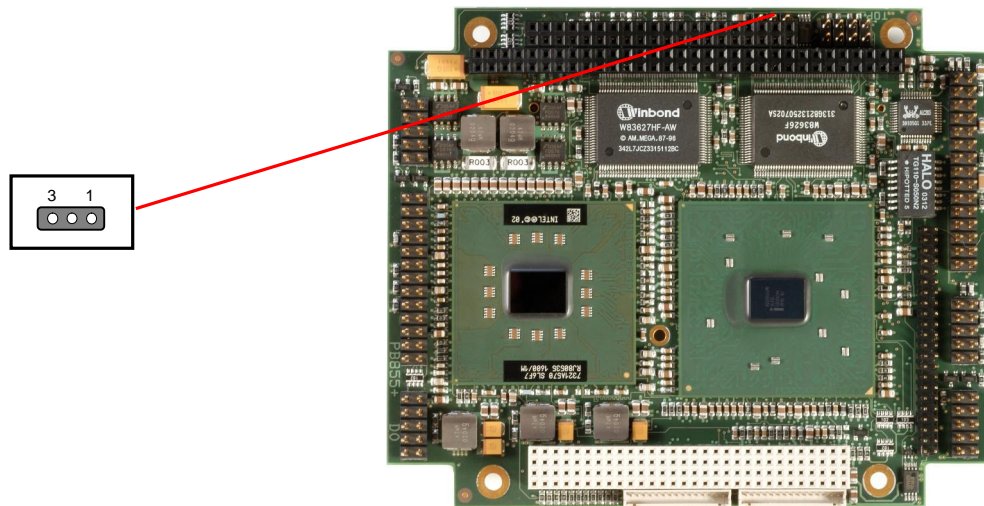


Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt

4.12 External Fan

This connector is for controlling and monitoring of a 5 volt fan.

For the monitoring the fan must provide a corresponding speed signal.



Pin	Name	Description
1	GND	ground
2	VCC	5V supply regulated
3	TACHO	Fan monitoring signal

5 BIOS Settings

5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.

This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.

See also the chapters [Load Fail-Safe Defaults](#) and [Load Optimized Defaults](#).

5.2 Top Menu

Phoenix - AwardBIOS CMOS Setup Utility	
<ul style="list-style-type: none"> ▶ Standard CMOS Features ▶ Advanced BIOS Features ▶ Advanced Chipset Features ▶ Integrated Peripherals ▶ Power Management Setup ▶ PnP/PCI Configuration ▶ PC Health Status 	<ul style="list-style-type: none"> ▶ Frequency/Voltage Control Load Fail-Save Defaults Load Optimized Defaults Set Password Save & Exit Setup Exit Without Saving
ESC: Quit ↑ ↓ → ← Select Item	
F10: Save & Exit Setup	
"brief description of selected item"	

The sign „►“ in front of a menu means that there is a sub menu.

The „x“ sign in front of a menu means, that there is an item which has to be enabled through the selection of another item.

5.3 Standard CMOS Features

Phoenix - AwardBIOS CMOS Setup Utility Standard CMOS Features		
Date (mm:dd:yy)	Mon, Jan 20 2002	Item Help
Time (hh:mm:ss)	11 : 11 : 00	
► IDE Primary Master	[None]	
► IDE Primary Slave	[None]	
► IDE Secondary Master	[None]	
► IDE Secondary Slave	[None]	
Drive A	[1.44M, 3.5in.]	
Video	[EGA/VGA]	
Halt On	[All, But Keyboard]	
Base Memory	640K	
Extended Memory	228352K	
Total Memory	229376K	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Date (mm:dd:yy)

Options: mm ... Month
 dd ... Day
 yy ... Year

ü Time (hh:mm:ss)

Options: hh ... Hours
 mm ... Minutes
 ss ... Seconds

ü IDE Primary Master

Sub menu: IDE Primary/Secondary Master/Slave

ü IDE Primary Slave

Sub menu: IDE Primary/Secondary Master/Slave

ü IDE Secondary Master

Sub menu: IDE Primary/Secondary Master/Slave

ü IDE Secondary Slave

Sub menu: IDE Primary/Secondary Master/Slave

ü Drive A

Options: None / 360K , 5.25 in. / 1.2M , 5.25 in. / 720K , 3.5 in. / 1.44M, 3.5 in.
 / 2.88M, 3.5 in.

ü VIDEO

Options: EGA/VGA / CGA 40 / CGA 80 / Mono

ü Halt On

Options: All Errors / No Errors / All , But Keyboard / All , But Diskette / All , But Disk/Key

ü Base Memory

Options: none

Ü Extended Memory

Options: none

Ü Total Memory

Options: none

5.3.1 IDE Primary/Secondary Master/Slave

Phoenix - AwardBIOS CMOS Setup Utility
IDE Primary Master

IDE HDD Auto-Detection	[Press Enter]	Item Help
IDE Primary Master	[Auto]	
Access Mode	[Auto]	
Capacity	0 MB	
Cylinder	0	
Head	0	
Precomp	0	
Landing Zone	0	
Sector	0	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü IDE HDD Auto-Detection

Options: none

ü IDE Primary Master

Options: Auto / None / Manual

ü Access Mode

Options: Auto / CHS / LBA / Large

ü Capacity

Options: none

ü Cylinder

Options: none

ü Head

Options: none

ü Precomp

Options: none

ü Landing Zone

Options: none

ü Sector

Options: none

5.4 Advanced BIOS Features

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

		Item Help
► CPU Feature	[Press Enter]	
Virus Warning	[Disabled]	
CPU L1 & L2 Cache	[Enabled]	
Quick Power On Self Test	[Enabled]	
First Boot Device	[Floppy]	
Second Boot Device	[HDD-0]	
Third Boot Device	[LS120]	
Boot Other Device	[Enabled]	
Boot Up Floppy Seek	[Enabled]	
Boot Up NumLock Status	[On]	
Gate A20 Option	[Normal]	
Typematic Rate Setting	[Disabled]	
x Typematic Rate (Chars/Sec)	6	
x Typematic Delay (Msec)	250	
Security Option	[Setup]	
APIC Mode	[Enabled]	
MPS Version Control For OS	[1.4]	
OS Select For DRAM > 64MB	[Non OS2]	
Report No FDD For WIN 95	[No]	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü CPU Feature

Sub menu: CPU Feature

ü Virus Warning

Options: Enabled / Disabled

ü CPU L1 & L2 Cache

Options: Enabled / Disabled

ü Quick Power On Self Test

Options: Enabled / Disabled

ü First Boot Device

Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / HDD-2 / HDD-3 / ZIP100 /
USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

ü Second Boot Device

Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / HDD-2 / HDD-3 / ZIP100 /
USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

ü Third Boot Device

Options: Floppy / LS120 / HDD-0 / SCSI / CDROM / HDD-1 / HDD-2 / HDD-3 / ZIP100 /
USB-FDD / USB-ZIP / USB-CDROM / USB-HDD / LAN / Disabled

ü Boot Other Device

Options: Enabled / Disabled

ü Boot Up Floppy Seek

Options: Enabled / Disabled

ü Boot Up NumLock Status

Options: Off / On

ü Gate A20 Option

Options: Normal / Fast

ü Typematic Rate Setting

Options: Enabled / Disabled

ü Typematic Rate (Chars/Sec)

Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

ü Typematic Delay (Msec)

Options: 250 / 500 / 750 / 1000

ü Security Option

Options: Setup / System

ü APIC Mode

Options: Enabled / Disabled

ü MPS Version Control For OS

Options: 1.1 / 1.4

ü OS Select For DRAM > 64MB

Options: Non-OS2 / OS2

ü Report No FDD For WIN 95

Options: No / Yes

ü Full Screen LOGO Show

Options: Enabled / Disabled

5.4.1 CPU Feature

Phoenix - AwardBIOS CMOS Setup Utility

CPU Features		
Thermal Management	[Thermal Monitor 2]	Item Help
TM2 Bus Ratio	[8 X]	
TM2 Bus VID	[1.180V]	
CPU Speed and Voltage	[Default]	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Thermal Management

Options: Thermal Monitor 1 / Thermal Monitor 2

ü TM2 Bus Ratio

Options: 6 ... 16¹

ü TM2 Bus VID

Options: 0.700 ... 1.484¹

ü CPU Speed and Voltage

Options: Pentium M 1,6GHz
1.4 GHz-1.420 V
1.2 GHz-1.276 V
1.0 GHz-1.164 V
800 MHz-1.036 V
600 MHz-0.956 V
Pentium M 1,1GHz
1.0 GHz-1.164 V
900 MHz-1.100 V
800 MHz-1.020 V
600 MHz-0.956 V
Pentium M 900MHz
800 MHz-0.988 V
600 MHz-0.844 V

¹ The maximal value depends on the CPU

5.5 Advanced Chipset Features

Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features

DRAM Timing Selectable	[By SPD]	Item Help
x CAS Latency Time	2	
x Active to Precharge Delay	6	
x DRAM RAS# to CAS# Delay	3	
x DRAM RAS# Recharge	3	
DRAM Data Integrity Mode	Non-ECC	
MGM Core Frequency	[Auto Max 266MHz]	
System BIOS Cacheable	[Disabled]	
Video RAM Cacheable	[Disabled]	
Memory Hole at 15M-16M	[Disabled]	
Delayed Transaction	[Enabled]	
Delay Prior to Thermal	[16 Min]	
AGP Aperture Size	[64]	
** On-Chip VGA Setting **		
On-Chip VGA	[Enabled]	
On Chip Frame Buffer Size	[32MB]	
Boot Display	[LFP]	
Panel Scaling	[Off]	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü DRAM Timing Selectable

Options: By SPD / Manual

ü CAS Latency Time

Options: 2.5 / 2

ü Active to Precharge Delay

Options: 5 / 6 / 7

ü DRAM RAS# to CAS# Delay

Options: 2 / 3

ü DRAM RAS# Recharge

Options: 2 / 3

ü DRAM Data Integrity Mode

Options: Non-ECC / ECC

ü MGM Core Frequency

Options: Auto Max 266MHz /
400/266/133/200 MHz /
400/200/100/200 MHz /
400/200/100/133 MHz /
400/266/133/167 MHz /
400/333/166/250 MHz /
Auto Max 400/333MHz

ü System BIOS Cacheable

Options: Enabled / Disabled

ü Video RAM Cacheable

Options: Enabled / Disabled

ü Memory Hole at 15M-16M

Options: Enabled / Disabled

ü Delayed Transaction

Options: Enabled / Disabled

ü Delay Prior to Thermal

Options: 4 Min / 8 Min / 16 Min / 32Min

ü AGP Aperture Size

Options: 4 / 8 / 16 / 32 / 64 / 128 / 256

ü On-Chip VGA

Options: Enabled / Disabled

ü On Chip Frame Buffer Size

Options: 1MB / 4MB / 8MB / 16MB / 32MB

ü Boot Display

Options: VBIOS Default / CRT / LFP / CRT+LFP

ü Panel Scaling

Options: Auto / On / Off

ü Panel NumberOptions:
640*480
800*600
1024*768
1280*1024
1400*1050
1600*1200

5.6 Integrated Peripherals

Phoenix - AwardBIOS CMOS Setup Utility		
Integrated Peripherals		
▶ OnChip IDE Device	[Press Enter]	Item Help
▶ Onboard Device	[Press Enter]	
▶ SuperIO Device	[Press Enter]	

ü OnChip IDE Device

Sub menu: OnChip IDE Device

ü Onboard Device

Sub menu: Onboard Device

ü SuperIO Device

Sub menu: SuperIO Devices

5.6.1 OnChip IDE Device

Phoenix - AwardBIOS CMOS Setup Utility				
OnChip IDE Device				
On-Chip Primary PCI IDE	[Enabled]	Item Help		
IDE Primary Master PIO	[Auto]			
IDE Primary Slave PIO	[Auto]			
IDE Primary Master UDMA	[Auto]			
IDE Primary Slave UDMA	[Auto]			
On-Chip Secondary PCI IDE	[Enabled]			
IDE Secondary Master PIO	[Auto]			
IDE Secondary Slave PIO	[Auto]			
IDE Secondary Master UDMA	[Auto]			
IDE Secondary Slave UDMA	[Auto]			
IDE HDD Block Mode			[Enabled]	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü On-Chip Primary PCI IDE

Options: Enabled / Disabled

ü IDE Primary Master PIO

Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

ü IDE Primary Slave PIO

Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

ü IDE Primary Master UDMA

Options: Disabled / Auto

ü IDE Primary Slave UDMA

Options: Disabled / Auto

ü On-Chip Secondary PCI IDE

Options: Enabled / Disabled

ü IDE Secondary Master PIO

Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

ü IDE Secondary Slave PIO

Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

ü IDE Secondary Master UDMA

Options: Disabled / Auto

ü IDE Secondary Slave UDMA

Options: Disabled / Auto

ü IDE HDD Block Mode

Options: Enabled / Disabled

5.6.2 Onboard Device

Phoenix - AwardBIOS CMOS Setup Utility		
Onboard Device		
USB Controller	[Enabled]	Item Help
USB 2.0 Controller	[Enabled]	
USB Keyboard Support	[Disabled]	
USB Mouse Support	[Disabled]	
AC97 Audio	[Auto]	
Init Display First	[Onboard/AGP]	
◀F2▶: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

ü USB Controller

Options: Enabled / Disabled

ü USB 2.0 Controller

Options: Enabled / Disabled

ü USB Keyboard Support

Options: Enabled / Disabled

ü USB Mouse Support

Options: Enabled / Disabled

ü AC97 Audio

Options: Disabled / Auto

ü Init Display First

Options: Onboard/AGP /
PCI Slot

5.6.3 SuperIO Devices

Phoenix - AwardBIOS CMOS Setup Utility
SuperIO Device

Onboard FDC Controller	[Enabled]	Item Help
Parallel Port Floppy	[Disabled]	
Onboard Serial Port 1	[3F8/IRQ4]	
Onboard Serial Port 2	[2F8/IRQ3]	
UART Mode Select	[Normal]	
x RxD , TxD Active	Hi,Lo	
x IR Transmission Delay	Enabled	
x UR2 Duplex Mode	Half	
Onboard Parallel Port	[378/IRQ7]	
Parallel Port Mode	[EPP]	
EPP Mode Select	[EPP1.9]	
x ECP Mode Use DMA	3	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü Onboard FDC Controller

Options: Enabled / Disabled

ü Parallel Port Floppy

Options: Enabled / Disabled

ü Onboard Serial Port 1

Options: Disabled /
3F8/IRQ4 /
2F8/IRQ3 /
3E8/IRQ4 /
2E8/IRQ3 /
Auto

ü Onboard Serial Port 2

Options: Disabled /
3F8/IRQ4 /
2F8/IRQ3 /
3E8/IRQ4 /
2E8/IRQ3 /
Auto

ü UART Mode Select

Options: Normal / ASKIR / IrDA

ü RxD , TxD Active

Options: Hi,Hi
Hi,Lo
Lo,Hi
Lo,Lo

ü IR Transmission Delay

Options: Enabled / Disabled

ü UR2 Duplex Mode

Options: Half / Full

ü Onboard Parallel Port

Options: 378/IRQ7 /
 278/IRQ5 /
 3BC/IRQ7

ü Parallel Port Mode

Options: SPP / EPP / ECP / ECP+EPP / Normal

ü EPP Mode Select

Options: EPP1.9 / EPP1.7

ü ECP Mode Use DMA

Options: 1 / 3

5.7 Power Management Setup

Phoenix - AwardBIOS CMOS Setup Utility		
Power Management Setup		
ACPI function	[Enabled]	Item Help
Power Management	[User Define]	
Video Off Method	[DPMS]	
Video Off in Suspend	[No]	
Suspend Type	[PwrOn Suspend]	
x Modem Use IRQ	3	
Suspend Mode	[Disabled]	
HDD Power Down	[Disabled]	
Wake-Up by PCI card	[Disabled]	
Power On by Ring	[Disabled]	
* Reload Global Timer Events *		
Primary IDE 0	[Disabled]	
Primary IDE 1	[Disabled]	
Secondary IDE 0	[Disabled]	
Secondary IDE 1	[Disabled]	
FDD,COM,LPT Port	[Disabled]	
PCI PIRQ[A-D]#	[Disabled]	
◀•: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

ü ACPI function

Options: Enabled / Disabled

ü Power Management

Options: User Define / Min Saving / Max Saving

ü Video Off Method

Options: Blank Screen / V/H SYNC+Blank / DPMS supported

ü Video Off in Suspend

Options: No / Yes

ü Suspend Type

Options: Stop Grant / PwrOn Suspend

ü MODEM Use IRQ

Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

ü Suspend Mode

Options: Disable / 1 Min / 2 Min / 4 Min / 8 Min / 12Min / 20 Min / 30 Min / 40 Min / 1 Hour

ü HDD Power Down

Options: Disable / 1 Min ... 15 Min

ü Wake-Up by PCI card

Options: Enabled / Disabled

ü Power On by Ring

Options: Enabled / Disabled

ü Primary IDE 0

Options: Enabled / Disabled

ü Primary IDE 1

Options: Enabled / Disabled

ü Secondary IDE 0

Options: Enabled / Disabled

ü Secondary IDE 1

Options: Enabled / Disabled

ü FDD,COM,LPT Port

Options: Enabled / Disabled

ü PCI PIRQ[A-D]#

Options: Enabled / Disabled

5.8 PNP/PCI Configuration

Phoenix - AwardBIOS CMOS Setup Utility

PNP/PCI Configuration

Reset Configuration Data	[Disabled]	Item Help
Resources Controlled By	[Auto(ESCD)]	
x IRQ Resources	[Press Enter]	
PCI/VGA Palette Snoop	[Disabled]	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- ü **Reset Configuration Data**
Options: Enabled / Disabled
- ü **Resources Controlled By**
Options: Auto(ESCD) / Manual
- ü **IRQ Resources**
Sub menu: IRQ Resources
- ü **PCI/VGA Palette Snoop**
Options: Enabled / Disabled

5.8.1 IRQ Resources

Phoenix - AwardBIOS CMOS Setup Utility

IRQ Resources

			Item	Help
IRQ-3	assigned to	[PCI Device]		
IRQ-4	assigned to	[PCI Device]		
IRQ-5	assigned to	[PCI Device]		
IRQ-7	assigned to	[PCI Device]		
IRQ-9	assigned to	[PCI Device]		
IRQ-10	assigned to	[PCI Device]		
IRQ-11	assigned to	[PCI Device]		
IRQ-12	assigned to	[PCI Device]		
IRQ-14	assigned to	[PCI Device]		
IRQ-15	assigned to	[PCI Device]		

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

ü IRQ-3 assigned to

Options: PCI Device / Reserved

ü IRQ-4 assigned to

Options: PCI Device / Reserved

ü IRQ-5 assigned to

Options: PCI Device / Reserved

ü IRQ-7 assigned to

Options: PCI Device / Reserved

ü IRQ-9 assigned to

Options: PCI Device / Reserved

ü IRQ-10 assigned to

Options: PCI Device / Reserved

ü IRQ-11 assigned to

Options: PCI Device / Reserved

ü IRQ-12 assigned to

Options: PCI Device / Reserved

ü IRQ-14 assigned to

Options: PCI Device / Reserved

ü IRQ-15 assigned to

Options: PCI Device / Reserved

5.9 PC Health Status

Phoenix - AwardBIOS CMOS Setup Utility

PC Health Status

Shutdown Temperature	[Disabled]	Item Help
Temp. Board	50°C	
Temp. CPU	34°C	
CPU Core	1.15V	
GMCH Core	1.16V	
CPU VTT	1.02V	
Memory 2.5V	2.49V	
+3.3V	3.29V	
+5V	4.99V	
VBatt	3.00V	
Fan1 Speed	5400 RPM	

<Esc>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

- ü Shutdown Temperature
- Options: Disabled /
60°C/140°F
65°C/149°F
70°C/158°F

- ü Temp. Board
- Options: None

- ü Temp. CPU
- Options: None

- ü CPU Core
- Options: None

- ü GMCH Core
- Options: None

- ü CPU VTT
- Options: None

- ü Memory 2.5V
- Options: None

- ü +3.3V
- Options: None

- ü +5.0V
- Options: None

- ü VBatt
- Options: None

- ü Fan1 Speed
- Options: None

5.10 Frequency/Voltage Control

Phoenix - AwardBIOS CMOS Setup Utility		
Frequency / Voltage Control		
Auto Detect PCI Clk	[Enabled]	Item Help
Spread Spectrum	[Disabled]	
<F2>: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

ü Auto Detect PCI Clk

Options: Enabled / Disabled

- Spread Spectrum

Options:

Disabled /
-0.25% /
-0.50% /
-0.75% /
-1.00% /
+/- 0.13%
+/- 0.25%
+/- 0.37%
+/- 0.50%

5.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.

At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.12 Load Optimized Defaults

This option applies like described under Load Fail-Safe Defaults.

At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.13 Set Password

Entry of passwords. (This causes most of the problems because passwords are often forgotten.)

5.14 Save & Exit Setup

Settings are saved and the board is restarted.

5.15 Exit without Saving

This option leaves the setup without saving any changes.

6 Software and Drivers

6.1 Drivers

The following table gives an overview of required and available drivers for some operating systems. If a required operating system is not listed and the installation of the operating system failed, please ask your distributor for a driver or another solution.



Attention

Please note, that you should install the latest service pack for the OS prior to driver installation.

Operating System	Chipset	VGA	USB	IDE	AC97	LAN
Windows 98/SE	CD	CD	CD	CD	CD	CD
Windows ME	CD	CD	CD	CD	CD	CD
Windows NT4	CD	CD	CD	CD	CD	CD
Windows 2000	CD	CD	CD	CD	CD	OS/CD ¹
Windows XP	CD	CD	CD	CD	CD	OS/CD ¹
Linux	OS	CD	OS	OS	CD	OS

OS Included in the operating system or no driver required.

CD A driver will be delivered on a CD.

6.2 BIOS-Update

The program “*AWDFLASH.EXE*” of the company Phoenix is used to update the BIOS. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “*EMM386.EXE*”. In case such a memory manager is loaded, the program will stop with an error message.

The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.

The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cd /cp
```

/sn Do not save the current BIOS

/cc Clear the CMOS

/cd Clear the DMI information

/cp Clear the PnP Information

The erasure of CMOS, DMI and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS.

A complete description of all valid parameters is shown with the parameter “/?”.

In order to make the BIOS run automatically, the parameter “/py” must be added. This parameter bypasses all security checks within the programming.

¹ A standard driver is included in the OS

7 Mechanical Drawing

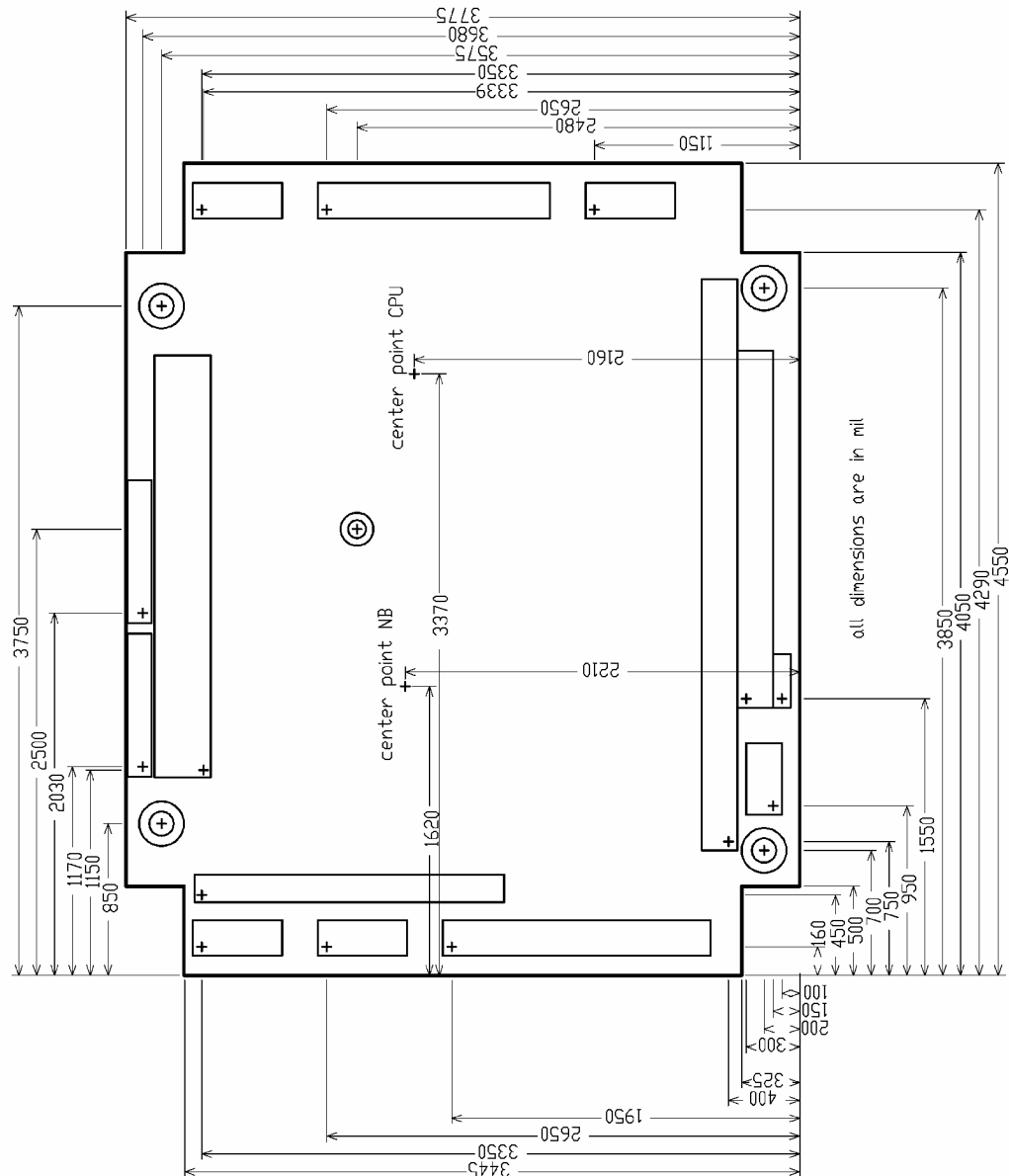
7.1 PCB

A true dimensioned drawing is included in the PC/104 Plus specifications.



Attention

All dimensions are in mil.

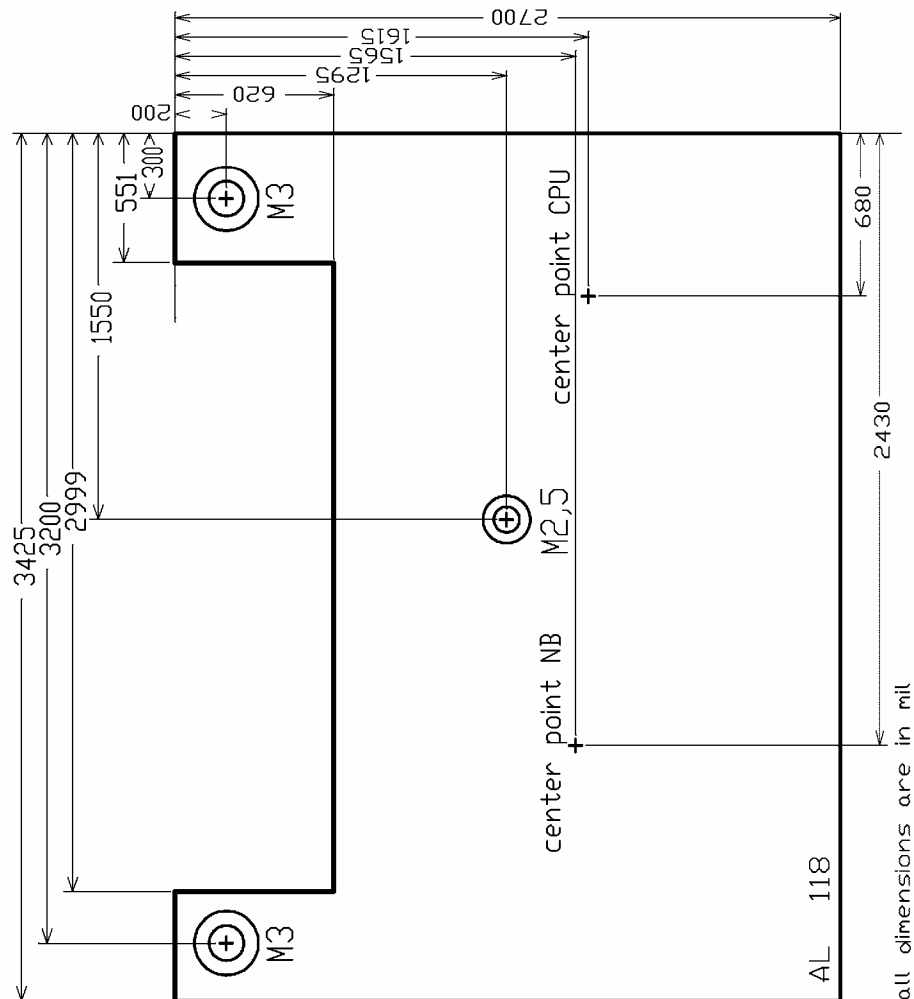


7.2 Heat spreader



Attention

All dimensions are in mil.



8 Technical Data

8.1 Electrical Data

Power Supply:

Board:	5 Volt +/- 5%
RTC:	≥ 3 Volt

Electric Power Consumption:

Board:	Pentium M 1,1GHz / 512MB => typical 1.8 A with 5V ¹ Pentium M 1,6GHz / 512MB => typical 2.6 A with 5V ¹
RTC:	≤ 10μA Environmental Conditions

8.2 Environmental Conditions

Temperature Range:

Operating:	0°C up to +60°C, extended on request
Storage:	0°C up to +60°C
Dispatch:	-20°C up to +70°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	0.5°C per minute
Dispatch:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85%, (non condensing)
Storage:	5% up to 95%, (non condensing)
Dispatch:	5% up to 100% for packaged boards, (non condensing)

Shock:

Operating:	150m/s, 6ms
Storage:	400m/s, 6ms
Dispatch:	400m/s, 6ms, for packaged boards

Vibrations:

Operating:	10 up to 58Hz, 0,075mm amplitude 58 up to 500Hz, 10m/s
Storage:	5 up to 9Hz, 2.5mm amplitude 9 up to 500Hz, 10m/s
Dispatch:	5 up to 9Hz, 3.5mm amplitude 9 up to 500Hz, 10m/s, for packaged boards

¹ The values were measured in Windows XP using standard software. PB855+ was connected to a PBEVA-S board. The harddisc was connected to a separate power supply. Maximum power consumption may be distinctly higher.

9 Thermal Specifications

The environmental temperature range is from 0°C to 60°C.

It has to be ensured that the DIE temperature of the processor does not exceed 100°C. The typical and the maximum power consumption must be considered. The maximum power consumption may be twice as much and should be used as a basis for the cooling concept.

Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.



Attention

The end customer has the responsibility to ensure that the DIE temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!

In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

I Annex Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyril or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - allot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed...
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program "write allocation" at AMD K5-CPU's.
4Eh	1. Program MTRR at M1 CPU's 2. Initialise level 2-cache at CPU's of the class P6 and set the "cacheable range" of the random access memory. 3. Initialise APIC at CPU's of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the "cacheable range" on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on "0")
55h	Only for multi processor systems (MP platform): Indicate the number of CPU's.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onboard_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM...
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the "chip set power management". 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PC's (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	<ol style="list-style-type: none"> 1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program "write allocation" at K6 CPUs (AMD) 7. Program "write combining" at P6 CPUs (INTEL)
95h	<ol style="list-style-type: none"> 1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	<ol style="list-style-type: none"> 1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex Resources

A IO-Range

The used resources depend on setup settings.

The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	IDE2
1F0-1F7	IDE1
278-27F	LPT2
2E8-3EF	COM4
2F8-2FF	COM2
370-377	FDC2
378-37F	LPT1
3BC-3BF	LPT3
3E8-3EF	COM3
3F0-3F7	FDC1
3F8-3FF	COM1

B Memory-Range

The used resources depend on setup settings.

If the USB boot function or legacy support is enabled, the BIOS uses 16KByte RAM in the range from A0000-FFFFF. If the entire range is clogged through option ROMs, these functions do not work any more.

Address	Function
A0000-BFFFF	VGA-RAM
C0000-CBFFF	VGA-Bios 48KByte
E0000-EFFFF	System-BIOS while booting
F0000-FFFFF	System-BIOS

C Interrupt

The used resources depend on setup settings.

The listed interrupts and their use are given through AT compatibility.

If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup. The exclusivity is not given and not possible on the PCI side.

Interrupt	Device
IRQ0	Timer
IRQ1	Keyboard
IRQ2 (9)	
IRQ3	COM1
IRQ4	COM2
IRQ5	
IRQ6	FDC
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	IDE Primary

Interrupt	Device
IRQ15	IDE Secondary

D PCI-Devices

All listed PCI devices exist on the board.

It is possible, that several PCI devices or functions of devices are disabled through setup settings in the BIOS.

AD	INTA	REQ	PCI	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge ID3580
	-	-	0	0	1	ID3584
	-	-	0	0	3	ID3585
	A	-	0	2	0	VGA Graphics ID3582
	-	-	0	2	1	Graphics Controller ID3582
	A	-	0	29	0	USB UHCI Controller #1 ID24C2
	D	-	0	29	1	USB UHCI Controller #2 ID24C4
	C	-	0	29	2	USB UHCI Controller #3 ID24C7
	H	-	0	29	7	USB 2.0 EHCI Controller ID24CD
	-	-	0	30	0	Hub Interface to PCI Bridge ID244E
	-	-	0	31	0	PCI to LPC Bridge ID24C0
	C	-	0	31	1	IDE Controller ID24CB
	B	-	0	31	3	SMBus Controller ID24C3
	B	-	0	31	5	AC '97 Audio Controller ID24C5
	B	-	0	31	6	AC '97 Modem Controller ID24C6
17	E	3	1	1	0	LAN Intel 82551ER ID1209
19	A	0	1	3		Externer Slot 1
20	B	1	1	4		Externer Slot 2
21	C	2	1	5		Externer Slot 3
22	D	3	1	6		Externer Slot 4
24	E	3	1	8	0	LAN intern ICH4 ID103A

E SMB-Devices

Address	Device
10-11	Standard slave address ICH4
60-61	Reserved from BIOS
88-89	BIOS defined slave address ICH4
A0-A1	SoDIMM200
A2-AF	Reserved from BIOS
D2-D3	ICS950813